REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

A new claim and claim amendments are presented herein to obviate the current rejection. No new matter has been added.

35 USC § 103

Claims 1, 5-7, 12, 16-18, 22, and 26-27 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over Pickreign in view of Saxena and in further view of Sharma. Claims 3-4, 8-11, 14-15, 19-21, 24-25, and 28-32 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over Pickreign in view of Saxena, and in further view of Sharma, and in yet further view of Shah. These rejections are respectfully traversed.

Claim 1 recites copying all contents of a memory of a network interface controller into a buffer in response to a first request to read information in the memory of the network interface controller. Claims 7, 12, 22, and 27 contain similar features.

Pickreign describes an arrangement in which a host computer requests to read data within its own memory space that is physically located within a network interface adapter (NIA) by

providing an address to the NIA processor via an address register (see, inter alia, Pickreign col. 3, lines 43-46). When the NIA processor is notified that the host computer is requesting to read data from an address within the host computer address space assigned to the NIA, the NIA processor translates that address to a physical address contained within the NIA address space (see, inter alia, Pickreign col. 3, lines 50-55). Using the address from the host computer, the NIA processor computes an offset from the assigned base address and uses this offset to locate the physical address of the data (see, inter alia, Pickreign col. 3, lines 61-65). Thereafter, the NIA processor transfers the data associated with the address to the host computer (see, inter alia, Pickreign col. 3, lines 65-67). Therefore, with Pickreign, only specifically requested data is transferred from the NIA processor to the host computer each time the host computer request to read data. Such an arrangement is inefficient and may cause unnecessary data traffic as compared to the claimed subject matter.

Saxena describes an arrangement in which a system responds to requests from an application by allocating storage for a data buffer, verifying that the application is authorized to access the buffer, converting an address of the buffer utilized by the application to a corresponding system address and mapping the system buffer address to an index (see, inter alia, Saxena

abstract). In response to subsequent transmit or receive requests, the system access the data buffer based on the index without requiring storage allocation, address conversion, or access verification (see, inter alia, Saxena abstract). Hence, Saxena is directed to a technique in which a device driver may access a data buffer within an application without address conversion delays.

Sharma describes an arrangement in which a memory controller selectively provides access to a plurality of agents, such as processors, cells of processors, I/O controllers and the like (see, inter alia, Sharma col. 3, lines 60-62). In a coherent mode, the memory controller ensures that an agent's cache reflects the most up to date data (see, inter alia, Sharma col. 3, line 62 - col. 4, line 5). In a read mode, a read-once segment of data is copied to an agent with the agent flushing the data upon completion of a transfer of the data to an external device (see, inter alia, Sharma col. 4, lines 5-26).

The skilled artisan would not have been motivated to combine the cited references to result in the claimed subject matter. Pickreign relates to a technique in which a host computer address space is mapped to a NIA address space to allow requested data to be transferred from the NIA to the host computer. Saxena also describes a mapping technique that allows access to a data buffer after an initial access without the need

for address conversion. Sharma, in contrast to both Pickreign and Saxena, describes a memory coherency technique that addresses problems associated with contending memory caches.

Neither of Pickreign or Saxena suggest that they be modified and combined in the manner proposed in the office action. Pickreign fails to suggest that buffer contents may be accessed. Saxena fails to suggest combining its subject matter with mirroring techniques, and in fact, the passage cited in the office action relates to a prior art system that is being distinguished by Saxena that pre-allocates a buffer. Furthermore, even if the skilled artisan were to combine Pickreign and Saxena, he or she would not have been motivated to additionally combine Sharma which relates to memory coherency issues with regard to a plurality of agent caches.

However, even if the references were combined, the skilled artisan would not have resulted in the claimed subject matter. None of the references suggest copying all contents of a memory of a network interface controller into a buffer in response to a first request to read information in the memory of the network interface controller. Pickreign describes a configuration in which only requested data is transferred from the NIA to the host computer. Saxena describes a mapping technique for address conversion purposes. Sharma describes a memory coherency

technique which is not initiated in response to a request to read information.

It is only with impermissible hindsight that the subject matter of the cited references is interpreted to render claim 1 unpatentable as the references fail to suggest the copying of all contents of a memory in response to a request to read information in the memory.

Accordingly, claims 1, 7, 12, 22, 27, and their respective dependent claims should be allowable.

Claim 18 recites a processor that is configured to "recopy the contents of the network interface controller memory into the buffer when packet traffic on the bus is below a predetermined level and if the contents of the network interface controller memory are modified" (see for support, inter alia, specification page 3, line 19 to page 4, line 2). None of the cited references suggest a processor that recopies the contents of a NIC memory when packet traffic on a bus is below a predetermined level.

Accordingly, claim 18 and its respective dependent claims should be allowable.

Claim 33 recites determining, in response to a second request to read information in the memory of the network interface controller, whether the contents of the memory of the network interface controller have been modified, copying all

contents of the memory of the network interface controller into the buffer if the contents have been modified, and accessing the contents of the buffer to read the information requested in the second request (see for support, inter alia, specification page 6, lines 15-23). Claim 33 should be separately allowable because none of the references suggest such a determination and subsequent copying of all contents of a memory.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Attorney's Docket No.:10559-386001

Applicant asks that all claims be allowed. Please apply $50 for the excess claim charges to our Deposit Account along with any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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